

N and P Channel 30V MOSFET

GENERAL DESCRIPTION

The JY12M is the N and P Channel logic enhancement mode power field transistors are produced using high cell density DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching, and low in-line power loss are needed in a very small outline surface mount package.

FEATURES

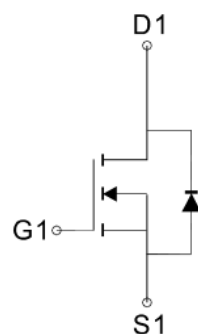
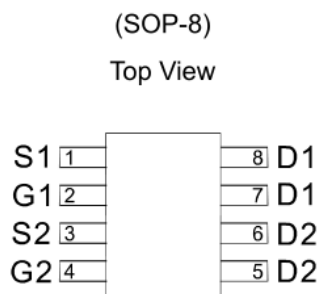
Device	$R_{DS(ON) MAX}$	$I_{D MAX}(25^{\circ} C)$
N-Channel	$20m\Omega @ V_{GS}=10V$	8.5A
	$32m\Omega @ V_{GS}=4.5V$	7.0A
P-Channel	$45m\Omega @ V_{GS}=-10V$	-5.5A
	$85m\Omega @ V_{GS}=-4.5V$	-4.1A

- Low Input Capacitance
- Fast Switching Speed

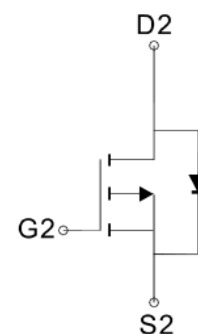
APPLICATIONS

- Power Management
- DC/DC Converter
- DC Motor Control
- LCD TV & Monitor Display Inverter
- CCFL inverter

PIN CONFIGURATION



N-Channel MOSFET



P-Channel MOSFET

JY12M

Absolute Maximum Ratings(Ta=25° C Unless Otherwise Noted)

Parameter		Symbol	N Channel		P Channel		Unit
			10 sec	Steady	10 sec	Steady	
Drain Source Voltage		V_{DSS}	30		-30		V
Gate Source Voltage		V_{DSS}	± 20		± 20		
Continuous Drain Current	Ta=25 °C	I_D	8.5	6.5	-7.0	-5.3	A
	Ta=70 °C		6.8	5.1	-5.5	-4.1	
Pulsed Drain Current		I_{DM}	30		-30		
Maximum Power Dissipation	Ta=25 °C	P_D	1.5				W
	Ta=70 °C		0.95				
Operating Junction Temperature		T_J	-55 to 150				°C
Thermal Resistance Junction to Ambient		$R_{\theta JA}$	61	100	62	103	°C/W
Thermal Resistance Junction to Case		$R_{\theta JC}$	15		15		°C/W

Electrical Characteristics(Ta=25° C Unless Otherwise Noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
Static							
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	N-Ch	1.0	1.5	3.0	V
		$V_{DS}=V_{GS}, I_D=-250\mu A$	P-Ch	-1.0	-1.5	-3.0	
I_{GSS}	Gate Leakage Current	$V_{DS}=0V, V_{GS}=\pm 20V$	N-Ch			± 100	nA
			P-Ch			± 100	
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=30V, V_{GS}=0V$	N-Ch			1	uA
		$V_{DS}=-30V, V_{GS}=0V$	P-Ch			-1	
$I_{D(ON)}$	On-State Drain Current	$V_{DS}\geq 5V, V_{GS}=10V$	N-Ch	20			A
		$V_{DS}\leq -5V, V_{GS}=-10V$	P-Ch	-20			
$R_{DS(ON)}$	Drain-Source On-State Resistance	$V_{GS}=10V, I_D=7.4A$	N-Ch		15	20	mΩ
		$V_{GS}=-10V, I_D=-5.2A$	P-Ch		38	45	
		$V_{GS}=4.5V, I_D=6.0A$	N-Ch		23	32	
		$V_{GS}=-4.5V, I_D=-4.0A$	P-Ch		65	85	
V_{SD}	Diode Forward Voltage	$I_S=1.7A, V_{GS}=0V$	N-Ch		0.8	1.2	V
		$I_S=-1.7A, V_{GS}=0V$	P-Ch		-0.8	-1.2	

Electrical Characteristics(Ta=25°C Unless Otherwise Noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Dynamic						
Qg	Total Gate Charge	N-Channel V _{DS} =15V,V _{GS} =10V, I _D =10A P-Channel V _{DS} =-15V,V _{GS} = -10V,I _D =-6A	N-Ch		9.8	nC
			P-Ch		10.5	
Qgs	Gate-Source Charge		N-Ch		1.6	
			P-Ch		1.8	
Qgd	Gate-Drain Charge		N-Ch		2.0	
			P-Ch		1.9	
Ciss	Input Capacitance	N-Channel V _{DS} =15V,V _{GS} =0V, f=1MHz P-Channel V _{DS} =-25V,V _{GS} =0V, f=1MHz	N-Ch		501	pF
			P-Ch		590	
Coss	Output Capacitance		N-Ch		72	
			P-Ch		69	
Crss	Reverse Transfer Capacitance		N-Ch		57	
			P-Ch		53	
Rg	Gate Resistance	V _{DS} =0V,V _{GS} =0V, f=1MHz	N-Ch		1.84	Ω
			P-Ch		11	
rrT _{d(on)}	Turn-On Delay Time	N-Channel V _{DD} =15V,V _{GS} =10V, R _G =6Ω,I _D =1A P-Channel V _{DD} =-15V,V _{GS} =-10 V, R _G =6Ω,I _D =-1A	N-Ch		3.9	ns
			P-Ch		6.8	
T _r	Turn-On Rise Time		N-Ch		4.2	
			P-Ch		4.9	
T _{d(off)}	Turn-Off Delay Time		N-Ch		16.6	
			P-Ch		28.4	
T _f	Turn-Off Fall Time	N-Ch		5.5		
		P-Ch		12.4		
T _{rr}	Reverse Recovery Time	I _F =12A, di/dt=500A/us	N-Ch		5.5	ns
			P-Ch		14	
Q _{rr}	Reverse Recovery Charge		N-Ch		2.6	nC
			P-Ch		11	

*The device mounted on 1in2 FR4 board with 2oz copper.

*Guaranteed by design. Not subject to product testing.

Typical Characteristics ($T_J=25^\circ\text{C}$ Noted)

N-Channel

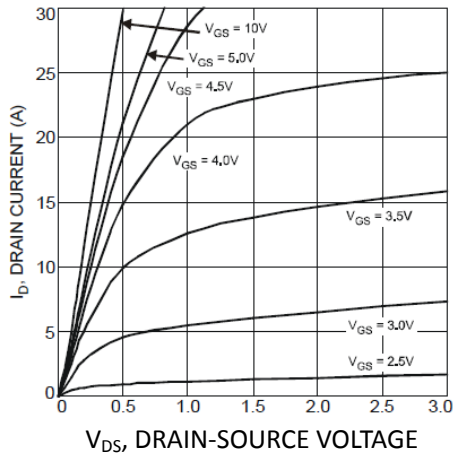


Figure1. Typical Output Characteristic

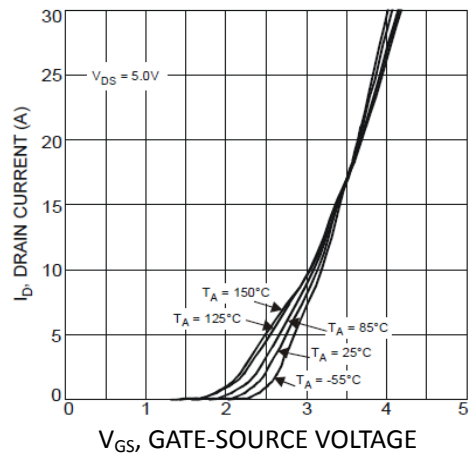


Figure2. Typical Transfer Characteristic

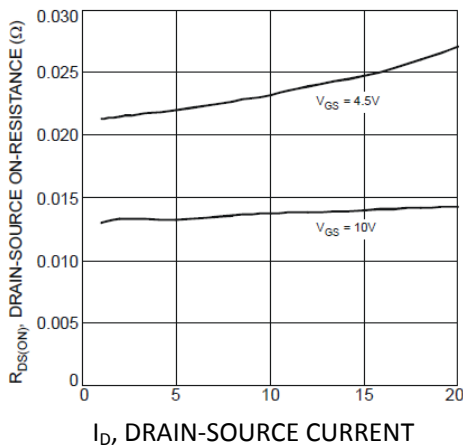


Figure3. Typical On-Resistance vs. Drain Current and Gate Voltage

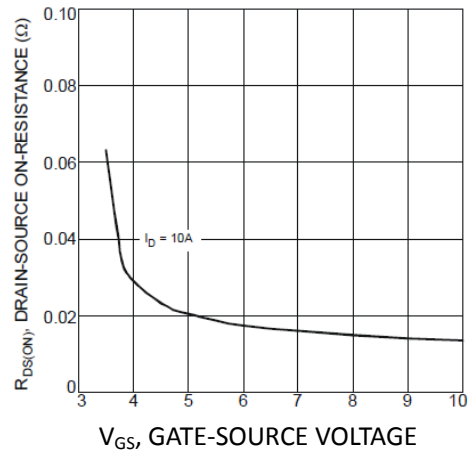


Figure4. Typical On-Resistance vs. Drain Current and Gate Voltage

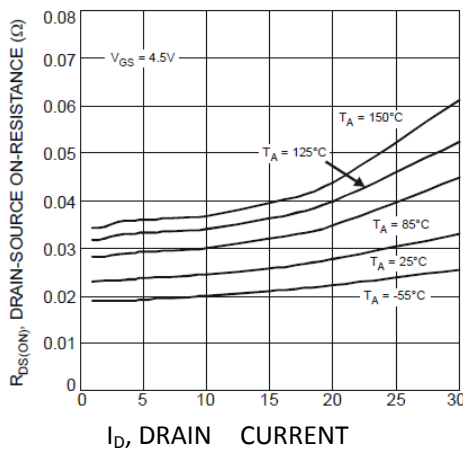


Figure5. Typical On-Resistance vs. Drain Current and Temperature

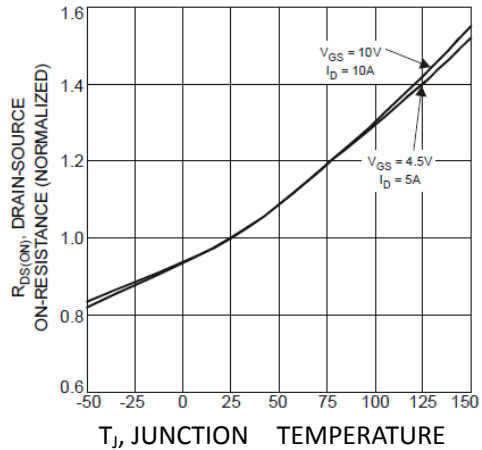


Figure6. On-Resistance Variation with Temperature

Typical Characteristics ($T_J=25^\circ\text{C}$ Noted)

N-Channel

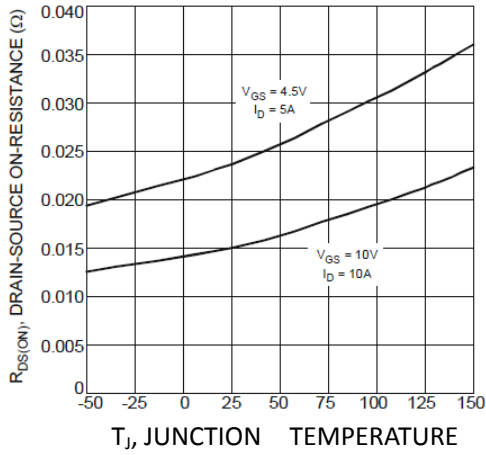


Figure 7. On-Resistance Variation with Temperature

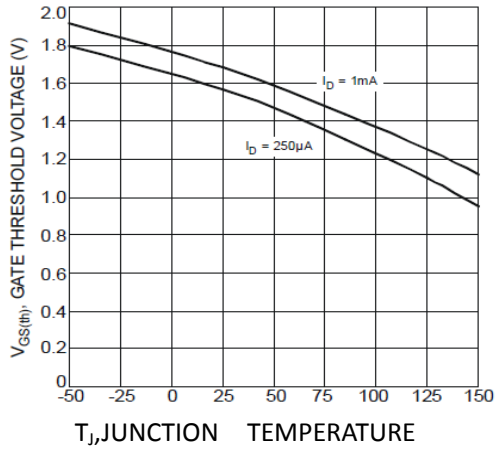


Figure 8. Gate Threshold vs. Ambient Temperature

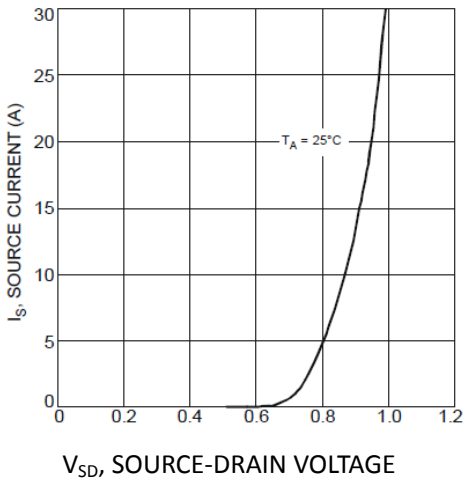


Figure 9. Diode Forward Voltage vs. Current

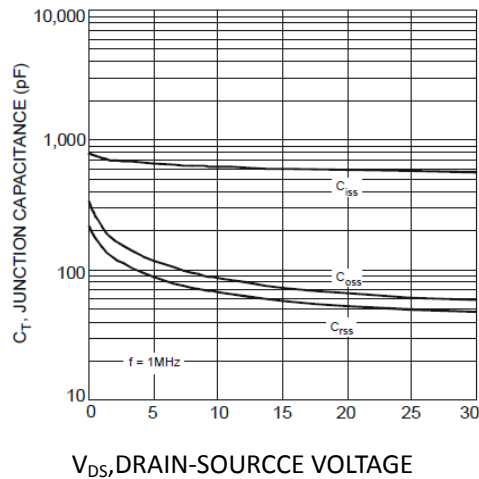


Figure 10. Typical Junction Capacitance

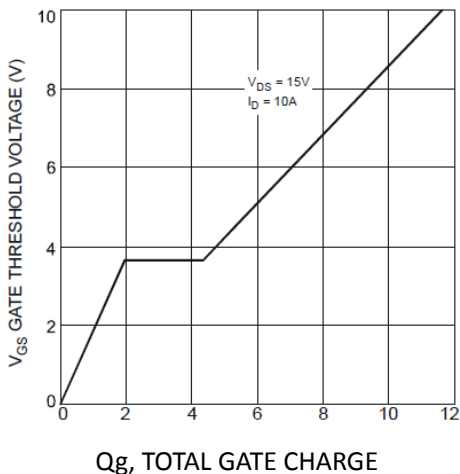


Figure 11. Gate Charge

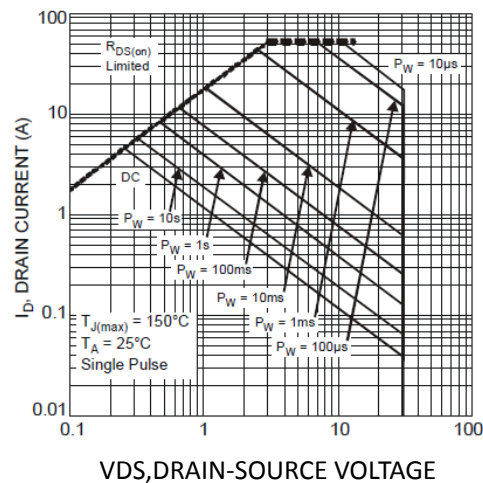


Figure 12. SOA, Safe Operation Area

Typical Characteristics ($T_J = 25^\circ\text{C}$ Noted)

P-Channel

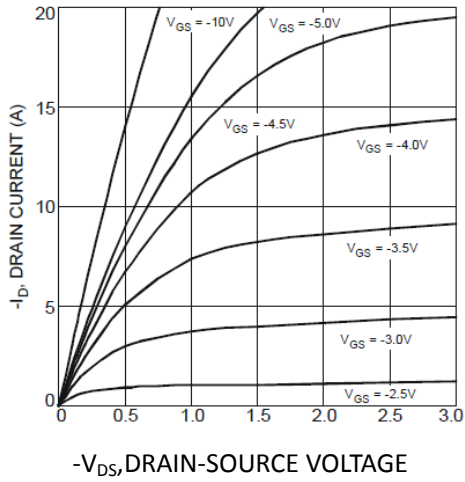


Figure 13. Typical Output Characteristics

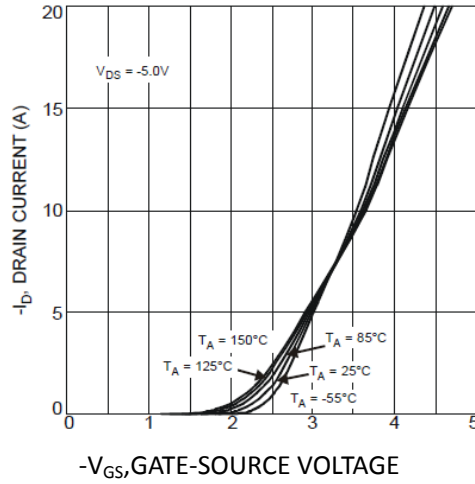


Figure 14. Typical Transfer Characteristics

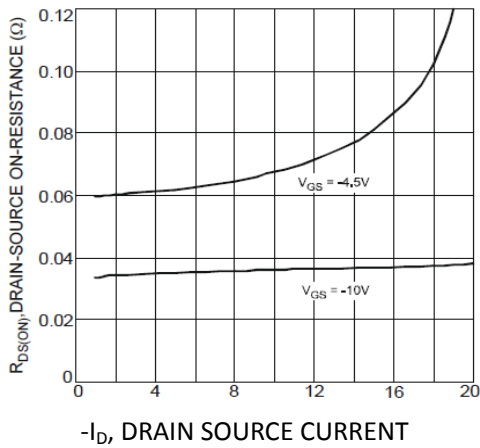


Figure 15. Typical On-Resistance vs. Drain Current and Gate Voltage

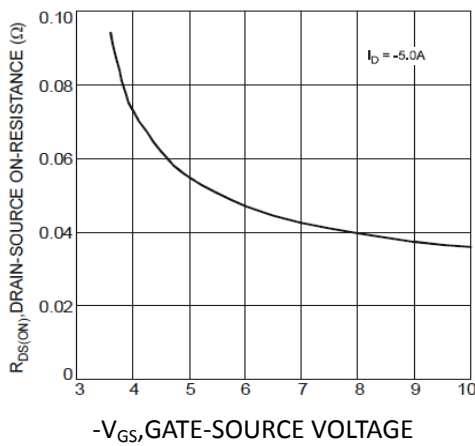


Figure 16. Typical On-Resistance vs. Drain Current and Gate Voltage

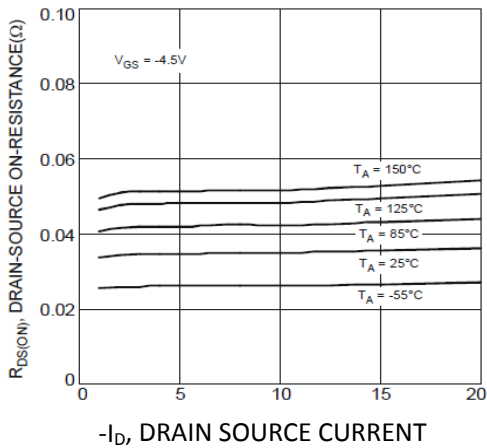


Figure 17. Typical On-Resistance vs. Drain Current and Temperature

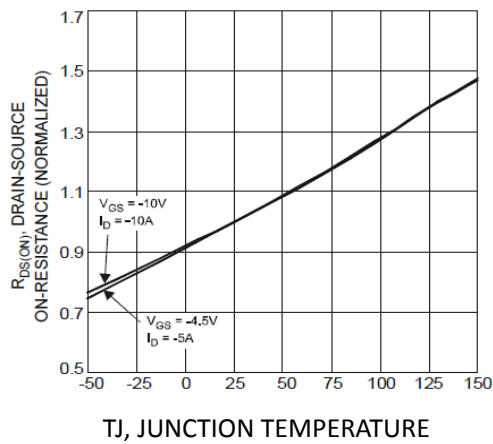


Figure 18. On-Resistance Variation with Temperature

Typical Characteristics ($T_J = 25^\circ\text{C}$ Noted)

P-Channel

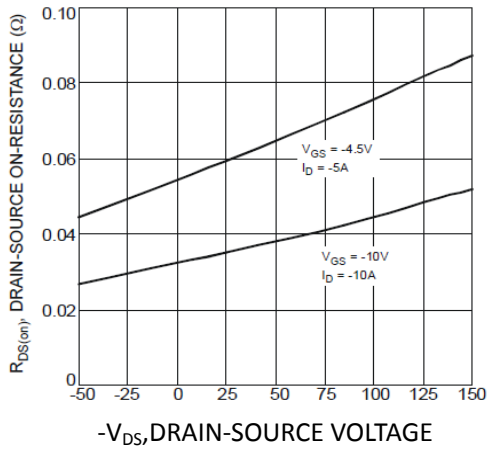


Figure 19. On-Resistance Variation with Temperature

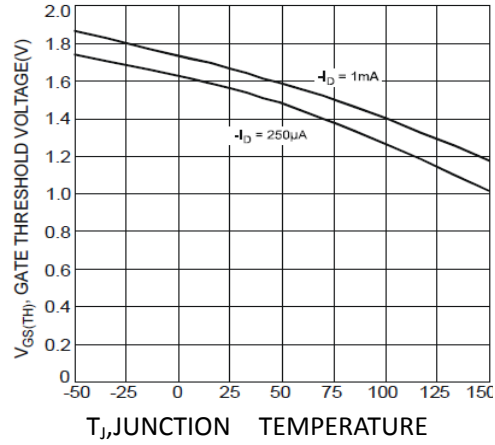


Figure 20. Gate Threshold vs. Ambient Temperature

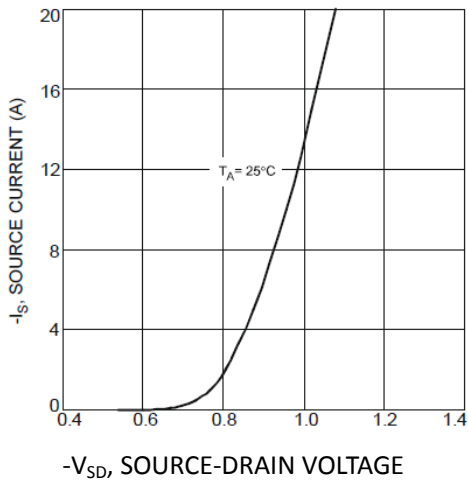


Figure 21. Diode Forward Voltage vs. Current

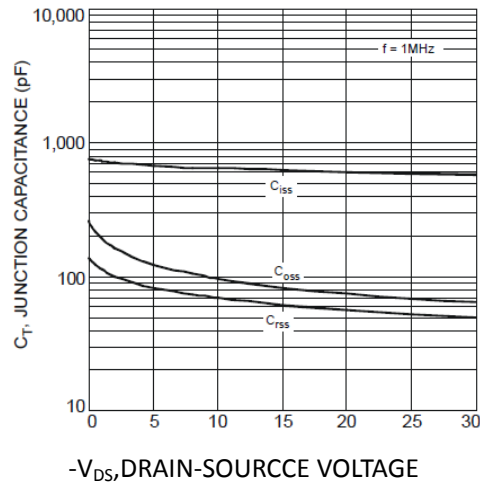


Figure 22. Typical Junction Capacitance

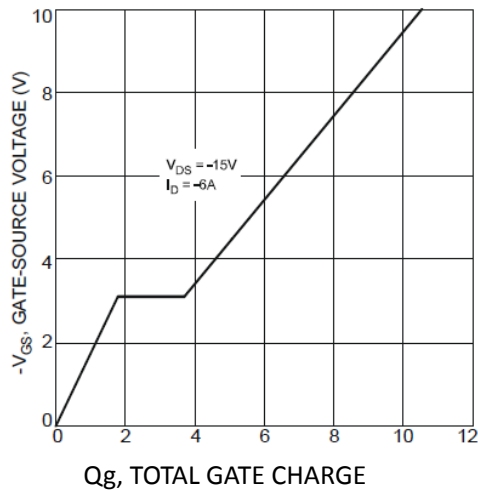


Figure 23. Gate Charge

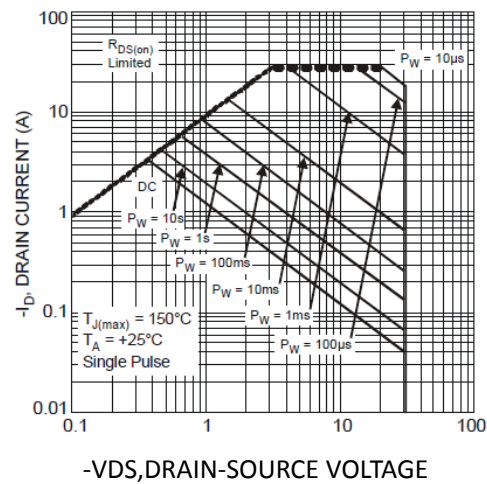
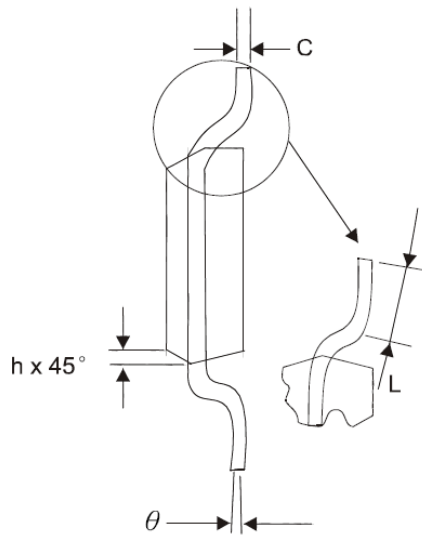
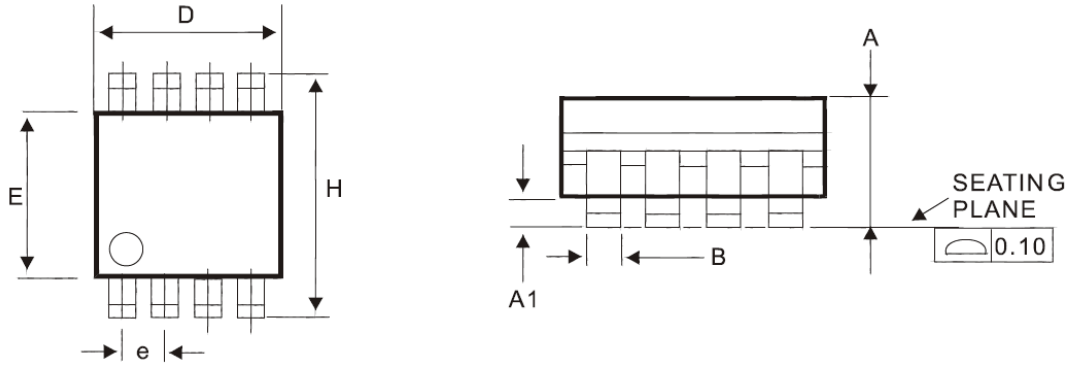


Figure 24. SOA, Safe Operation Area

SOP-8 Package Outline



DIM	MILLIMETERS	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.18	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
θ	0°	7°